REMARKS

Reconsideration of the present application is respectfully requested. Claims 28-32 and 34-36 are currently pending. No claims have been canceled, amended, or added.

Claims 28-30 and 34-36 have been allowed. Applicant wishes to thank the Examiner for the allowance of claims 28-30 and 34-36.

Claims 31 and 32 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,783,998 to Nakajou et al. ("Nakajou"). Nakajou describes a battery pack including a secondary battery coupled to an electronic device to behave as a power source of the electronic device. The battery pack is described by Nakajou as including a plus terminal (EB+) and a minus terminal (EB-) for supplying a current to the electronic device, a communication terminal (DATAB) for exchanging data with the electronic device, and a connection terminal (BATTINB) connected to the electronic device when the plus terminal and the minus terminal are properly connected to the electronic device.

Regarding claims 31 and 32, the Office Action asserts that column 5, lines 58-67 of Nakajou disclose "a) the claimed current source providing a current value, which is met by charge current flowing along the path of the processor 11A form the load/charger 11 (electronic device), (b) the claimed processor configured to calculate a resistance in the battery responsive to the current value and voltage drop value at an input to the electronic device, which is met by processor 11A determining if a certain level of voltage is applied to the gate of FET3, then the ON resistance becomes small, and the voltage drop at the source and the drain is small." The Office Action further asserts that column 4, lines 36-52 of Nakajou disclose "c) the claimed circuitry for enabling communication of data between the processor and the battery, which is met by data supplied through the data terminal DATAB, CPU 1." Applicant respectfully submits that Nakajou fails to teach or suggest at least the feature of independent claim 31 of "a processor configured to calculate a resistance in the battery responsive to the current value and a voltage drop value at an input to the electronic device."

Column 4, lines 36-52 of Nakajou describe that, in response to data supplied through the data terminal DATAB, CPU 1 executes predetermined processing or delivers information on the current status of the secondary battery E through the data terminal B. Column 5, lines 58-67

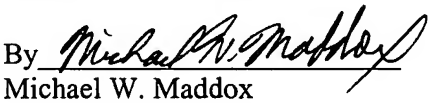
of Nakajou describe that when the load/charger 11 is set to operate as a battery charger, a charge current begins to charge the secondary battery E. Nakajou further describes that if a certain level of voltage is supplied to the gate of FET3, the ON resistance becomes small and the voltage drop at the source and drain is small. Even if these statements of Nakajou are assumed, for the sake of argument, to be true, Nakajou still fails to teach or suggest a processor configured to calculate a resistance in a battery responsive to a current value and a voltage drop value at an input of an electronic device as found in independent claim 31. Applicant respectfully submits that independent claim 31 distinguishes over Nakajou and requests that the 35 U.S.C. 102(b) rejection of independent claim 31 be withdrawn.

Claim 32 is dependent upon and includes the features of independent claim 1. For at least the reasons as discussed above with respect to independent claim 31, Applicant respectfully submits that claim 32 also distinguishes over Nakajou and requests that the 35 U.S.C. 102(b) rejection of claim 32 be withdrawn.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

Dated: March 28, 2005

Respectfully submitted,

By 

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